

Application No. 09/729,882
Page 3 of 5

REMARKS

Claims 1-3 and 5-25 remain pending in the application. Claim 1, the only independent claim, has been amended herein. Claim 1 has been amended to remove the 35 U.S.C. 112, first paragraph, raised by the Examiner by incorporation of the subject matter of claim 4, which is also given in the Specification on page 4, lines 25-28 and page 9, lines 6-7. While applicants believe that the previously use phrase "without eroding", although not explicitly used, is proper and is supported by the specification; applicants delete this phrase and submit that the current amendment clarifies what is claimed. A marked-up copy of the amendment showing the changes which have been made is attached to this Response.

Claims 1-3 and 5-25 remaining in the application have been rejected under 35 U.S.C. §102(b) as being anticipated by, or, in the alternative, under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,049,978 to Bates et al. The rejection is traversed.

With regard to applicants' claim 1 as amended, Bates, column 5, lines 38, does teach the use of a metal layer and a photoresist (masks). However, in Bates the photoresist material has been completely removed prior to the etching step as described in column 5, lines 24-27 and lines 32-34. Specifically, at column 5, lines 24-27, Bates states that the unilluminated photoresist is removed. At lines 33-35, Bates describes removing the remaining photoresist material. Consequently, when the plasma etching ("predetermined dry gas" in applicants' parlance) is carried out as described by Bates in lines 35 *et seq.*, only one mask is present. Nowhere in Bates is there an indication of two masks being present during the "gas" etching step.

In contrast to Bates, in Applicant's invention both the metal layer and the photoresist are present during the etching step using a predetermined etching gas as stated in Applicants' specification, for example, on page 4, lines 24-28, and again on 9, lines 11-12. Since Bates specifically teaches against the presence of both masks during the gas etching step, Applicants respectfully submit that claim 1, as amended, is allowable over the cited art with regard to both the anticipation and obviousness rejections. Further, Applicants respectfully submit that claims 2-3 and 5-25, all of which are directly or indirectly dependent on claim 1, are allowable for being dependent on an allowable claim.

In view of the foregoing difference between the cited art and the present invention as now claimed, Applicants respectfully submit that it is proper for the Examiner to withdraw the §102(b) and §103(a) rejections of the claimed invention and to allow the applicant to proceed to issue as a patent.

Application No. 09/729,882
Page 4 of 5

Applicants' undersigned attorney of record requests that the Examiner call if there are any matters whose resolution will facilitate prosecution of the application.

19 May 2003
Date

CERTIFICATE OF TRANSMISSION UNDER 37 C.F.R. § 1.8	
I hereby certify that this paper and any papers referred to herein are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9311 on:	
<u>19 May 2003</u> Date	
<u>Walter M. Douglas</u> Walter M. Douglas	<u>19 May 2003</u> Date

Respectfully submitted,
CORNING INCORPORATED

Walter M. Douglas

Walter M. Douglas
Registration No. 34,510
Corning Incorporated
Patent Department
Mail Stop SP-TI-03-1
Corning, NY 14831
Phone: (607) 974-2431
Fax: (607) 974-3848

Sheet Showing Amendment to Claims filed Herewith

1. (twice amended) A method for manufacturing an integrated optical circuit on a substrate, the substrate having a first region and a second region distinct from the first region, the method comprising the steps of:

forming a first mask on the substrate, the first mask defining a pattern corresponding to at least one optical device to be formed in the first region of the substrate;

forming a second mask on the substrate, the second mask defining a pattern corresponding to an optical structure to be formed in the second region of the substrate; and

etching the substrate having simultaneously thereon the first and second masks, ~~without eroding said first and second masks,~~ in order to form at least one optical device and the optical structure on the substrate

wherein said etching comprises using a predetermined etching gas, and said first and second masks are made of a material which substantially resists the predetermined etching gas.



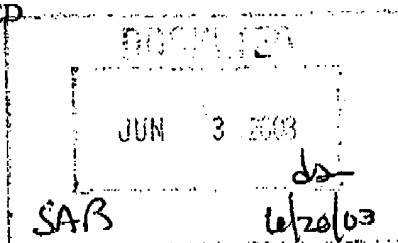
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/729,882	12/05/2000	Jean-Charles J.C. Cottéverte	Cottéverte 2-1-1-1	6768

22928 7590 05/30/2003

CORNING INCORPORATED
SP-TI-3-1
CORNING, NY 14831



EXAMINER
KUNEMUND, ROBERT M

ART UNIT	PAPER NUMBER
1765	9

DATE MAILED: 05/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

m4-9

Advisory Action	Application No. 09/729,882	Applicant(s) COTTEVERTE ET AL.	
	Examiner Robert M Kunemund	Art Unit 1765	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 19 May 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

(a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

(b) ☐ they raise the issue of new matter (see Note below);

(c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____

3. ☒ Applicant's reply has overcome the following rejection(s): 112 first paragraph.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____

Claim(s) objected to: _____

Claim(s) rejected: 1-25

Claim(s) withdrawn from consideration: _____

8. ☐ The proposed drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

10. ☐ Other: _____

ROBERT KUNEMUND
PRIMARY EXAMINER

Continuation Sheet (PTO-303)
09/729,882

Continuation of 5. does NOT place the application in condition for allowance because: the prior art does not require the removal of the masks, it is optional..

06/18/03 08:18:01

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Page 001

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Exhibit 4

Auto-Reply Facsimile Transmission



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<p>TO: Commissioner for Patents Attn: Examiner R. M. Kunamund Group Art Unit 1705</p>				
<p>FROM: Walter M. Douglas</p>				
<p>CC: [Redacted]</p>				
<p>Pages: 2 including Cover</p>				
<p>Fax No. 703-672-6211</p>				
<p>Date: June 18, 2003</p>				
<p>Re: US application 09/720,662 Ser. 125/00</p>				
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FROM:

Dr. Walter M. Douglas

Senior Patent Attorney

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Exhibit 4 pg 2

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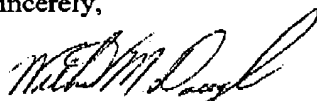
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To: Commissioner for Patents Attn: Examiner R. M. Kunemund Group Art Unit 1765	From: Walter M. Douglas
CC:	Pages: 2 Including Cover
Fax No. 703-872-9311	Date: June 18, 2003
Re: US application 09/729,882 filed 12/5/00	
Docket Number: Cotteverte, et al	
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Exhibit 4 pg. 3

Attorney Docket Number: Cotteverte 2

NOTICE OF APPEAL FROM THE PRIMARY EXAMINER
TO THE BOARD OF APPEALS

Inventor: Cotteverte, et al

Serial No: 09/729,882

Filing Date: December 5, 2000

Title: METHOD FOR MAKING AN
INTEGRATED OPTICAL
CIRCUIT

Examiner: Robert M. Kunemund

Group Art Unit: 1765

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal to the Board of Appeals from the Advisory Action decision dated May 20, 2003 of the Primary Examiner finally rejecting claims 1 - 25.

Corning Incorporated hereby authorizes to charge deposit account 03-3325 in the amount of \$320.

18 June 2003
Date

CERTIFICATE OF TRANSMISSION UNDER 37 C.F.R. § 1.8	
I hereby certify that this paper and any papers referred to herein are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9311 on:	
<u>18 June 2003</u> Date	
<u>Walter M. Douglas</u> Walter M. Douglas	<u>14 June 2003</u> Date

Respectfully submitted,
CORNING INCORPORATED

Walter M. Douglas
Walter M. Douglas
Registration No. 34,510
Corning Incorporated
Patent Department
Mail Stop SP-TI-03-1
Corning, NY 14831

Exhibit 5

Division SM Date 8/13/03
 INVENTOR Cottverre, et al
 CASE No. Cottverre, et al
 SERIAL No. 09/789,882
 FILED 12/5/00
 ATTORNEY WMO

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 CASE No. Cottverre, et al
 SERIAL No. 09/789,882
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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/782,802	
	Filing Date	12/12/2000	
	First Named Inventor	Cotteverte, et al	
	Group Art Unit	1765	
	Examiner Name	Robert K. Kunemund	
Total Number of Pages in This Submission	51	Attorney Docket Number	Cotteverte 2

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<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
<input type="checkbox"/> Amendment / Reply	<input type="checkbox"/> Licensing-related Papers	<input checked="" type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
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<input type="checkbox"/> Affidavits/declaration(s)	<input type="checkbox"/> Petition to Convert to a Provisional Application	<input type="checkbox"/> Status Letter
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EXB 5-P43
Attorney Docket No. Cotteverte 2RECEIVED
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: J.C. Cotteverte et al.

Serial No: 09/729,882

Filing Date: December 5, 2000

Title: METHOD FOR MAKING AN
INTEGRATED OPTICAL
CIRCUIT

Examiner: Robert K. Kunemund

Group Art Unit: 1765

OFFICIAL

Mail Stop: Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants respectfully submit this Brief to the Board of Patent Appeals and Interferences to appeal the final rejection dated March 20, 2003, of the above identified application. Appellants filed the Notice of Appeal on June 18, 2003, and now submit this Brief in triplicate, as required by 37 C.F.R. § 1.192(a). Appellants have also filed the appropriate petition and paid the required fee to gain an extension of the due date for filing this Brief to the Board. Please charge Deposit Account Deposit Account No. 03-3325 the \$320.00 fee under 37 CFR 1.17(c) for filing the Appeal Brief. If any extension of time under 37 C.F.R. § 1.136 is required to make the submission of this Appeal Brief timely, such an extension is requested and the fee should also be charged to our Deposit Account No. 03-3325.

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Corning Incorporated.

Exb. 5-09 4

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-3 and 5-25 remain in the application. These are the pending claims that are the subject of this Appeal and are set forth in the attached Appendix. Claim 1 has been amended twice. Claim 4 was cancelled in Appellants Response to the Final Office Action filed on May 19, 2003.

IV. STATUS OF AMENDMENTS

Appellants received an Advisory Action mailed May 30, 2003 advising: (1) that the 35 U.S.C. §112, first paragraph, rejection was overcome; (2) that all claims remain rejected (under 35 U.S.C. §§ 102 and 103); and (3) that the last amendments to the claims would be entered for purposes of Appeal. Accordingly, in this Brief Appellants' reference to the claims 1-3 and 5-25 remaining in the application refer to the claims as of May 19, 2003. A complete set of claims 1-3 and 5-25 is attached hereto.

V. SUMMARY OF INVENTION

The present invention relates to a method for manufacturing an integrated optical circuit in which an optical device (for example, a waveguide, resonator, etc.) is associated with an array structure (for example, a frequency band gap region). In particular, the method comprises:

- forming on a face of a substrate a first mask that defines a pattern corresponding to at least one optical device to be formed in a first region of the substrate;
- forming on the face of the substrate a second mask defining a pattern corresponding to an optical structure to be formed in a second region of the substrate distinct from the first region; and
- etching the substrate having thereon the first and second masks in order to form the at least one optical device and the optical structure on the substrate.

Utilizing the foregoing method one is able to produce in a single step an integrated

optical structure on a substrate in accordance with the patterns set by the two masks. The patterns defined by the two masks are distinct from one another as set forth in claim 1 and in the specification at page 3, lines 10-16.

The novel feature of the invention is that the two masks are used simultaneously to produce an integrated optical circuit having different elements in different regions of a substrate in a simplified manner thus reducing costs. In addition, the method allows one to produce an integrated circuit with great accuracy. This is particularly important in the productions of integrated telecommunications circuits utilizing photonic crystals.

An example of such an integrated circuit is one have one or more optical devices such as waveguides, couplers, splitters and so forth, and an array structure such as one defining a photonic band gap proximate to the optical device. In such integrated circuits the optical device(s) and the array structure have quite different shapes. For example, the array structure may be periodic or quasi-periodic with a period that may be small (for example, ca. 200-250nm) whereas the device is not. A typical technique to prepare a mask suitable for making such periodic structure is interference lithography which uses two interfering laser beams. However, interference lithography is not suitable for forming a mask corresponding to optical devices (e.g., waveguides, couplers, etc.) because such devices do not consist of a periodic or quasi-periodic structure. These masks must be produced using a more conventional lithographic technique such as irradiation by UV (ultraviolet) light.

According to the invention one forms two different masks on a substrate. Each mask is directed to a different region of the substrate and is use to for different elements as described above. Once the masks are formed on the structure, a single technique such as etching can then be used to form the integrated circuit.

In contrast to the present invention, using a single mask for both an optical device and an optical structure would require a complicated lithographic method for producing the mask. Such method would have to be adapted to all the different types of shapes contained in the pattern to be created in the substrate. While the known UV and electron beam lithographic techniques are suitable for producing masks for waveguides, couplers and similar devices, at the present time they do not have sufficient accuracy for form array structures such as the photonic band gap mentioned above. Consequently, a better method as exemplified by the present invention is required

Exh. 5 pg 6
Attorney Docket No. Cotteverte 2

VI. ISSUES

Issues presented for consideration in this Appeal are:

A. Whether claims 1-3 and 5-25 are patentable under 35 U.S.C. §102 (b) as not being anticipated by U.S. Patent No. 5,049,978 to Bates et al. (hereinafter "Bates").

B. Whether claims 1-3 and 5-25 are patentable under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,049,978 to Bates et al. (hereinafter "Bates").

C. **NOTE:** Claim 1-25 were also rejected in the Final Office Action under 35 U.S.C. §112, first paragraph. However, this rejection was withdrawn in the Advisory Action issued in response to Appellants response after the Final office Action in which appellants entered amendments. Accordingly, since the Examiner indicated in the Advisory Action that amendments would be entered for purpose of appeal, the §112, first paragraph, rejection is not discussed herein.

VII. GROUPING OF CLAIMS

In compliance with 37 C.F.R. § 1.192(7), Appellants state that all of the claims stand or fall together. Claim 1 is the only independent claim in the application. Claims 2-3 and 5-25 depend on claim 1.

VIII. ARGUMENTS

A. The Examiner's Rejection. Claims 1-3 and 4-25

In the Final Office Action of March 30, 2003, the Examiner rejected pending claims 1-3 and 5-25 under 35 U.S.C. §102(b) as anticipated by, or in the alternative under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,049,978 to Bates et al.]. On pages 3 and 4 of the final Office Action, the Examiner stated that:

"The Bates et al reference teaches a conductively enclosed hybrid assembly. A substrate of silicon is provided (column 4, lines 38-42). Recesses are created in the substrate. A preferred etches [*sic*] for creating the recesses in the silicon substrate is plasma etch. The etch is patterned by a metal such as Cr, TiW, Ti, or Al. A first step in mask formation is the sputtering of an unpatterned metal of the plasma resistant metal covering the upper surface of the substrate (col 5, lines 15-21). This reads of the first masking step. The metal layer is then

patterned. The metal layer is covered with a photoresist, which is exposed to an optical pattern defining the recesses. The claimed second masking step. The region of the metal layer from which the photoresist has been removed are then exposed to an acid etch to create openings in the metal mask (col 5, lines 29-34). A solvent may remove the photoresist. The recesses support individual MMIC chips. The use of a silicon substrate has the further advantage of permitting efficient optical interconnection with optical circuits within the package while maintaining a hermetic seal col' 13, lines 15-20. The Bates et al reference does not teach that an optical device is formed in the first and second region of the substrate. However, the Bates et al. Reference teaches that MMIC chips are formed in the recess in the substrate. MMIC chips are optical devices. Thus it would have been obvious to one of ordinary skill in the art that Bates et al inherently teaches optical devices are formed in the substrate." [Sic.]

Applicant respectfully submits that the Examiner failed to provide a *prima facie* case of either anticipation or obviousness because:

- (a) With regard to anticipation, Bates does not teach the formation of two masks defining "a first and second pattern in distinct regions". Anticipation requires that a single reference teach each and every element of the claimed invention be present in the cited art as will be shown below, this does not occur in the Bates patent. I
- (b) With regard to obviousness, one of ordinary skill in the art would not be motivated to use or modify the teaching of Bates to obtain Applicant's invention because Bates neither teaches nor suggests that one can use two masks defining separate patterns. In re Vaeck, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991).

Ex. 5 pg 8
Attorney Docket No. Cotteverte 2

B. Appellant's Argument

The claimed invention is best understood by a review of the steps of Bates and comparing them with those of the claimed invention. While the Examiner attempted to summarize Bates in Section VIII A above, Appellants believe that summary is defective because it does not properly describe what Bates actually does. It is here noted that what Bates is seeking to do is to make recesses in the substrate into which MMIC chips, made elsewhere, can be inserted and subsequently bonded to a metallic layer. Bates does not use two masks to simultaneously form two different elements, for example a device and an array, on the surface of a substrate.

Where necessary to fully explain what is being taught, Appellants have entered and identified their comments.

(1) What Bates teaches is:

1. Providing a substrate (column 4, lines 38-42) into which the recesses are to be formed.
2. Applying an unpatterned metal layer to the substrate (column 5, lines 19-20).
 - **Appellants' Comment:** While one may argue that this layer is a mask, at this point it is unpatterned and defines no element or device in a distinct region of the substrate.
3. Covering the metal layer with a photoresist and subjecting the photoresist to an "optical pattern" that defines the recesses that are to be formed in the substrate (column 5, lines 22-24).
 - **Appellants' Comment:** The patent does not specify whether the "optical pattern" is in the form of a mask that is applied to the photoresist or is an image project onto the photoresist. Whichever the case may be, there are not two different patterns defining different areas of the substrate.
4. The photoresist is chemically developed and the polymerized area of the photoresist removed to expose the underlying metal layer (column 5, lines 24-29).
 - **Appellants' Comment:** At this point there is a single mask defining a single pattern; namely, photoresist layer having a part thereof removed to define the recesses that are to be made.

5. The metallic layer is then wet etched to remove the exposed metal and bare the substrate (column 5, lines 29-32). The undeveloped photoresist may then be removed (column 5, lines 32-34).

• **Appellants' Comment:** The Examiner has argued that after the wet etching there are two masks present on the substrate, one being the photoresist layer and the other being the metal layer. However, in Bates both define the same pattern in the same regions of the substrate and not different patterns in distinct regions of the substrate as Appellants are claiming.

6. After wet etching the patterned metal mask is subjected to a plasma etch to form the recesses in the substrate (Bates, column 5, lines 35-43).

7. When the plasma etching is completed and the recesses are formed the metal mask is removed (column 5, lines 56-57). The substrate surface is cleaned and metalized with (1) chromium, (2) nickel and (3) gold. The MMIC chips are then inserted into the recess and bonded to the gold layer.

• **Appellants' Comment:** The MMIC chips are formed elsewhere, inserted into the recesses and bonded to the gold layer. The MMIC chips are not formed in the substrate as the Examiner has stated in the Final Office Action. (See Bates, (See column 3, lines 1-9 and column 6, lines 2-5, both of which indicate that the MMIC chips are inserted into the substrate and bonded to a metallic layer.) Consequently, Appellants submit that the Examiner conclusion that Bates teaches the formation of optical devices in a substrate is erroneous.

In contrast to Bates, Appellants teach and claim a method for the formation of two separate "elements" in different regions of a substrate. The substrate is then etched in a single step and the two elements are formed as a result on this single etching step. Appellants steps are as follows. A copy of Appellants' Figures reference below is attached as Appendix B.

(2) What Appellants teach and claim.

1. A metal layer 8 and a first photoresist 9 are applied to a substrate 7. Substrate 7 consists of a silica base substrate 7a, a first thin silica layer 7b and a second thin silica layer 7c on top of layer 7b, where the refractive

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index of 7c is higher than that of 7b. (See the application, page 7, lines 22-28).

2. A silica mask, having a chromium pattern on its upper surface defining an optical waveguide to be formed in the substrate, is placed over to the photoresist layer 9 and resulting masked substrate exposed to UV radiation (application, page 7, line 29 to page 8, line 7).
3. The silica mask is removed and the photoresist layer 8 developed leaving only a portion of the photoresist layer 9a (Fig. 2C) having the same shape as the chromium pattern (application, page 8, lines 8-12).
4. The metal layer 8 is then wet etched to remove the metal not covered by the photoresist remaining on the substrate (application, page 8, lines 13-19). As a result of the wet etching the photoresist is then removed (application, page 8, lines 19-20). To form a metal mask 8a defining a pattern, in this case being a waveguide.
5. A second photoresist layer 11 is formed on substrate 7 and metal mask 8a (application, page 8, lines 21-27, and Fig. 2F).
6. Two interfering lasers are directed to the photoresist 11 to form a pattern such that after development of the photoresist a second pattern is formed, in this case the mask defining an array of holes to be formed. (See application, page 8, line 28 to page 9, line 5).

Appellants' comment: As per claim 1 and the specification on page 9, lines 5-6, at this point there are two masks present on the substrate.

These masks define different elements in different regions of the substrate. One is the waveguide and the second is the array. Both the photoresist and metal masks are resistant to dry etching (application, page 9, lines 6-7)

7. A dry etch is performed without eroding the two masks (application, page 9, lines 8-13).
8. The masks are removed to leave a waveguide and an array on the substrate (application, page 9, lines 14-22).

Appellants' comment: Note that Appellants do not require the insertion of a separately formed device into the substrate as is required by Bates.

Appellants submit that the above comparison clearly indicates that the Bates

patent does not teach the claimed invention. Bates does not teach the simultaneous use of two masks defining two different elements and/or devices in different regions of a substrate in a single forming step. There is no suggestion in Bates that such a procedure can be used. What Bates does do is form a recess in a substrate into which a device formed independently, the MMIC chip, can be inserted.

IX. CONCLUSION

In conclusion, in view of the comparisons, facts and arguments set forth above Appellants request requests a reversal of each of the grounds of rejection maintained by the Examiner and submit that the application and claims therein are allowable.

If there are any other fees due in connection with the filing of this Brief on Appeal, please charge the fees to our Deposit Account No. 03-3325. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for herein, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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Date: 13 August 2003

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The claims on appeal are as follows:

1. (previously amended) A method for manufacturing an integrated optical circuit on a substrate, the substrate having a first region and a second region distinct from the first region, the method comprising the steps of:

forming a first mask on the substrate, the first mask defining a pattern corresponding to at least one optical device to be formed in the first region of the substrate;

forming a second mask on the substrate, the second mask defining a pattern corresponding to an optical structure to be formed in the second region of the substrate; and

etching the substrate having simultaneously thereon the first and second masks in order to form the at least one optical device and the optical structure on the substrate,

wherein said etching comprises using a predetermined etching gas, and said first and second masks are made of a material which substantially resists the predetermined etching gas..

2. The method of claim 1 further comprising the step of:

removing the first mask and the second mask.

3. The method of claim 1 wherein the step of etching is dry etching using a predetermined etching gas.

4. (cancelled)

5. The method of claim 3 wherein the predetermined etching gas is a fluorine-bearing gas.

6. The method of claim 1 wherein the steps of forming the first mask and the second mask are carried out such that the first mask and the second mask overlay one another.

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7. The method of claim 6 wherein the first mask has a first portion which overlays the second mask and a second portion which is in direct contact with the substrate.

8. The method of claim 1 wherein one of the first mask or the second mask is formed using an interference lithography technique and the other of the first mask or the second mask is formed using a UV exposure technique.

9. The method of claim 1 wherein the second mask is formed using an interference lithography technique and radiation, and the first mask is made of a material which is substantially insensitive to the radiation used in the interference lithography technique, so that the second mask may be formed after the formation of the first mask without affecting the first mask.

10. The method of claim 9 wherein the step of forming the second mask comprises the steps of:

forming a photoresist layer on the substrate; and
forming a pattern corresponding to the optical structure in the photoresist layer using the interference lithography technique.

11. The method of claim 9 wherein the first mask is made of a metal and the second mask is made of a photoresist material.

12. The method of claim 11 wherein the first mask is made of a metal selected from the group consisting of nickel, chromium, or gold.

13. The method of claim 9 wherein the step of forming the first mask comprises the steps of:

forming a first layer on the substrate, the first layer being made of a material which is substantially insensitive to light;

forming a photoresist layer on the first layer;
patterning the photoresist layer using the UV exposure technique to obtain a photoresist pattern corresponding to the first region of the substrate;

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etching the first layer using the photoresist pattern as the first mask; and
removing the photoresist pattern.

14. The method of claim 13 wherein the step of etching the first layer is wet etching.

15. The method of claim 9 wherein the first mask and the second mask are both made of a photoresist material, the first mask being a photoresist material which has been heated to remove its sensitivity to light.

16. The method of claim 15 wherein the step of forming the first mask comprises the steps of:

forming a photoresist layer on the substrate;
patterning the photoresist layer using a UV exposure technique to obtain a
pattern corresponding to the first region of the substrate; and
heating the photoresist pattern to remove its sensitivity to light.

17. The method of claim 1 wherein the first mask is formed using a UV exposure technique and the second mask is made of a material which is substantially insensitive to UV radiation, so that the first mask may be formed after the formation of the second mask without affecting the second mask.

18. The method of claim 1 wherein the substrate is a silicon on insulator substrate.

19. The method of claim 1 wherein the optical structure is an array structure.

20. The method of claim 1 wherein the second region of the substrate is proximate to the first region.

21. The method of claim 20 wherein the array structure consists of a periodic array of irregularities.

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22. The method of claim 21 wherein the array structure defines a frequency band gap.
23. The method of claim 21 wherein the array structure is a periodic array of holes.
24. The method of claim 21 wherein the array structure is a periodic array of rods.
25. The method of claim 21 wherein the at least one optical device is a waveguide.

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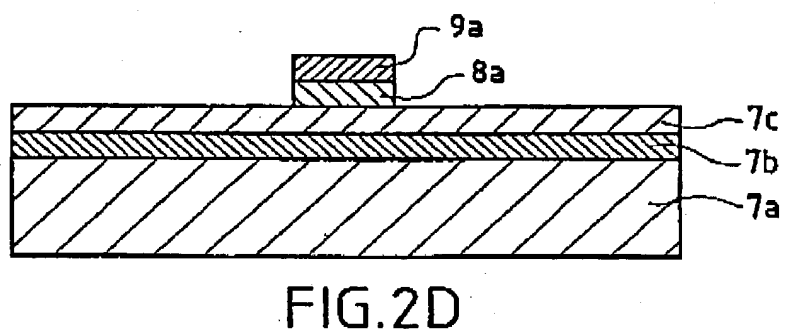
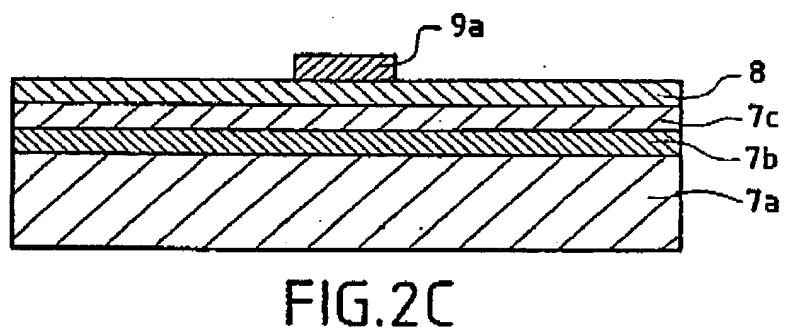
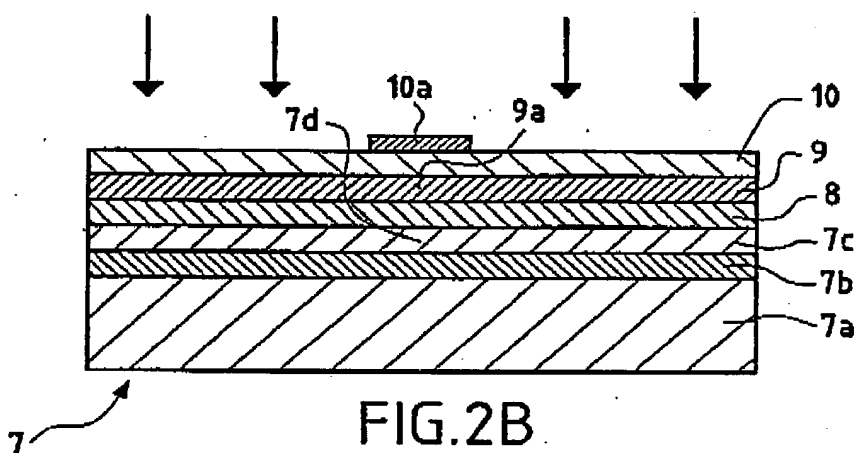
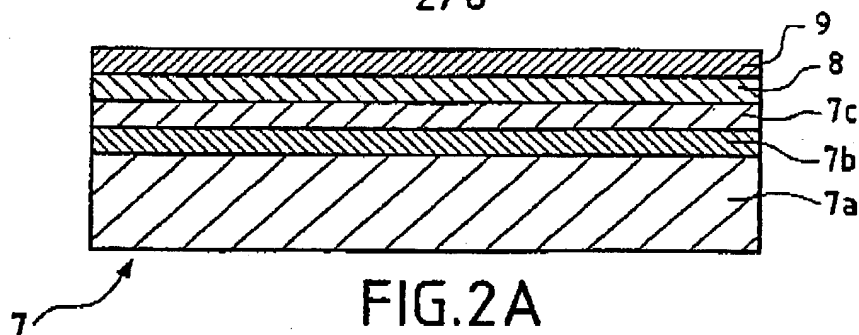
Attorney Docket No. Cottaverte 2

APPENDIX B TO BRIEF ON APPEAL

Figures 2A-2J referred to in the Brief are shown on the following pages.

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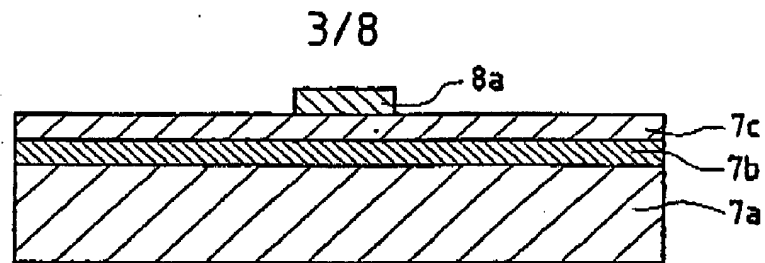


FIG.2E

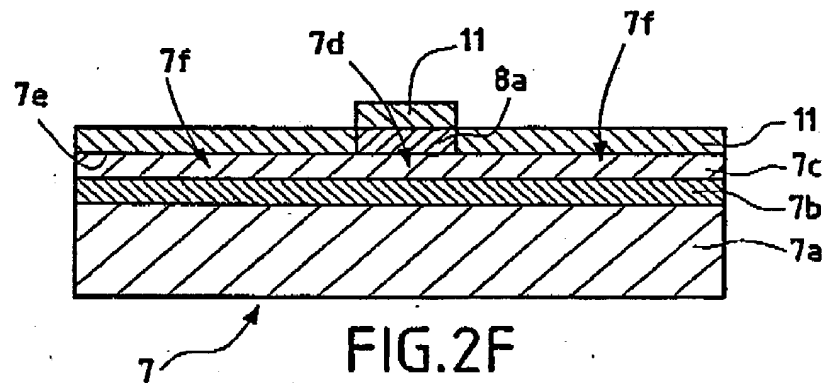


FIG.2F

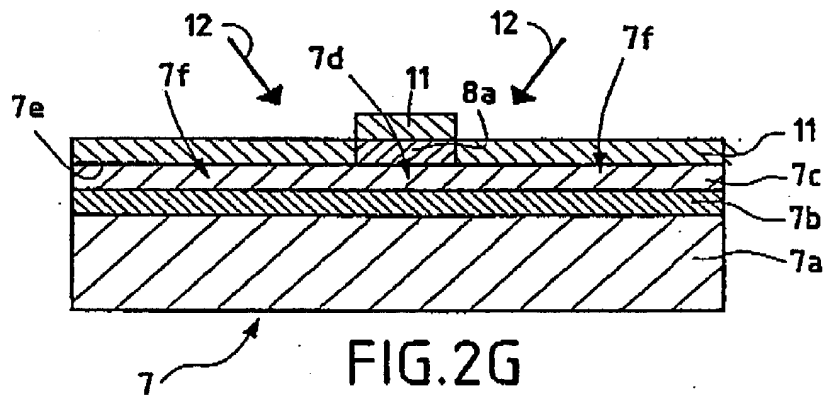


FIG.2G

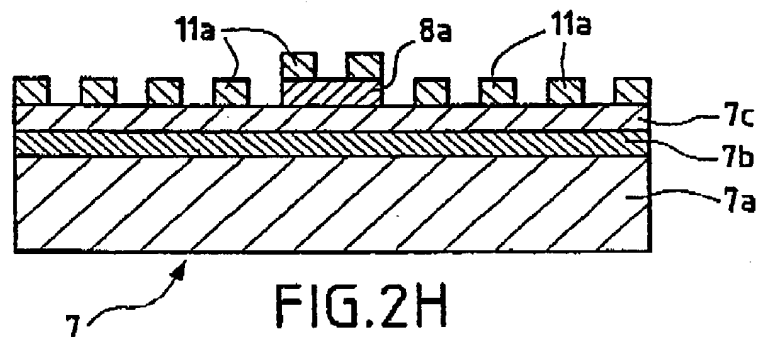


FIG.2H

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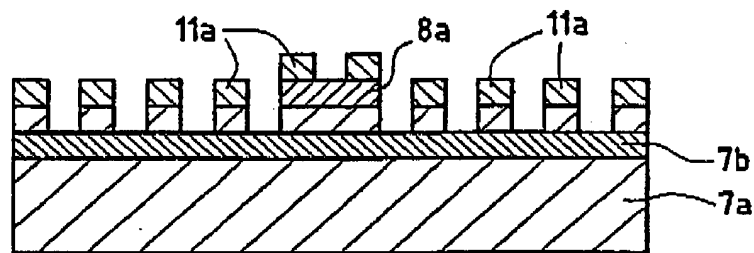


FIG. 2I

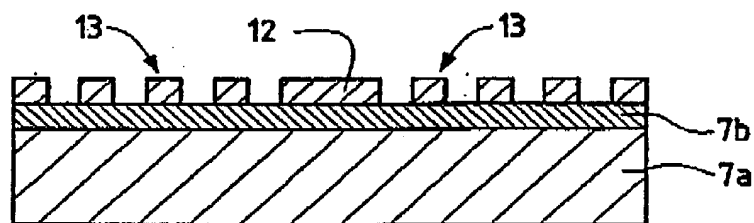


FIG. 2J

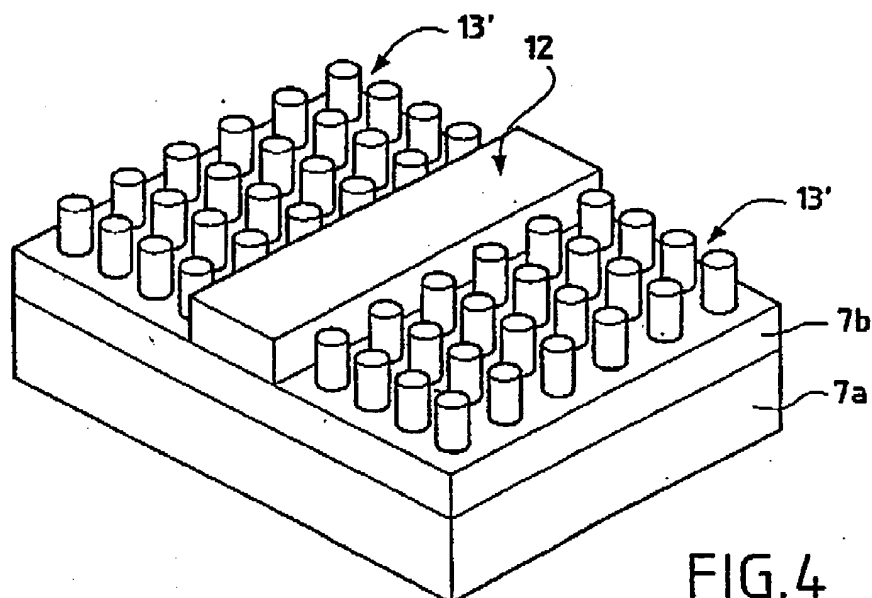


FIG. 4

*Exhibit 6***Gustin, Terri L**

From: Gustin, Terri L
Sent: Monday, January 19, 2004 3:13 PM
To: 'customerservice1700@uspto.gov'
Subject: Status of US 09/729882

Importance: High

Please provide the current status of the Appeal Brief filed 8/13/03. our docket number Cotteverte 2.

Thank you.

Terri L. Gustin

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Status Inquiry

Page 1 of 2

Gustin, Terri L**Exhibit 7**

From: Linda.Hodge-Taylor@uspto.gov
Sent: Tuesday, February 03, 2004 6:00 AM
To: GustinTL@corning.com
Cc: Nicol.Scott@uspto.gov
Subject: RE: Status Inquiry 09/729,882

PALM INTRANET**Application Number Information**Application Number: **09/729882** AssignmentsFiling Date: **12/05/2000**Effective Date: **12/05/2000**Application Received: **12/06/2000**Pat. Num./Pub. Num: **/20020074307**Issue Date: **00/00/0000**Date of Abandonment: **00/00/0000**Attorney Docket Number: **Cotteverte 2-1-1-1**Status: **120 /NOTICE OF APPEAL FILED**Confirmation Number: **6768**Title of Invention: **METHOD FOR MAKING AN INTEGRATED OPTICAL CIRCUIT**Examiner Number: **6502**Group Art Unit: **1765**Class/Subclass: **216/024**Lost Case: **NO**

Interference Number:

Unmatched Petition: **NO**L&R Code: **Secrecy Coc**Third Level Review: **NC**Oral Hearing: **NO**

Bar Code	PALM Location	Location Date	Charge to Loc	Charge
09729882	28C1	12/22/2003	No Charge to Location	No Charge

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Thanks in advance Nicky
Linda M. Hodge-Taylor
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Status Inquiry

Page 2 of 2

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-----Original Message-----

From: GustinTL@Corning.com [mailto:GustinTL@Corning.com]

Sent: Monday, February 02, 2004 3:01 PM

To: Customer Service 2800

Subject: Status Inquiry 09/729,882

PAIR show this case has been transferred to your group.

Could you please provide a status for the Appeal Brief that was filed August 13, 2003 via Express Mail.
US application No. 09/729,882 our docket number Cotteverte 2.

Thanks,

Terri

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